Design and Manufacturing Collaboration

Michael R. Creeden CEO/CID+

San Diego PCB, Inc. & EPTAC

mike.creeden@sdpcb.com

(858)271-5722

We will look at:

1. Why we collaborate?
2. When do we collaborate?
3. Who do we collaborate with?
4. What do we collaborate?

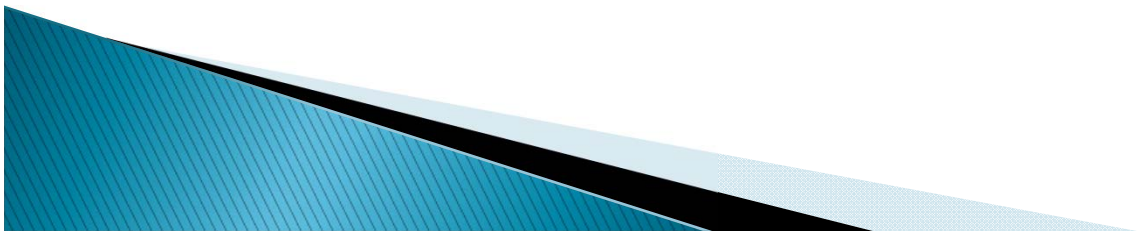
Why we collaborate?

- ***Every manufacturer I've ever known, are always encouraging us to be forward thinkers.***

"We can best do this by being prepared, planning ahead, to research and anticipate!"

******Therefore as designers we Collaborate******

- **Definition of *Collaborate*: to work with another person or group in order to achieve or do something**
- ***Our goal as designers is not to just design a board, but rather it's to design a board so that it can be built well!***



Why we collaborate?

- *Are your designs "Correct by construction?"*
- *How many boards do you manufacture? ####*

  …unless you're a manufacturer, the answer is 0.000
- *Qualify your vendor: visit, learn their process, learn their capabilities, speak their language, build a relationship, know the person*
- *Do you know the build plan – proto to prod.?*
- *Do you proto-type where you build production runs?*

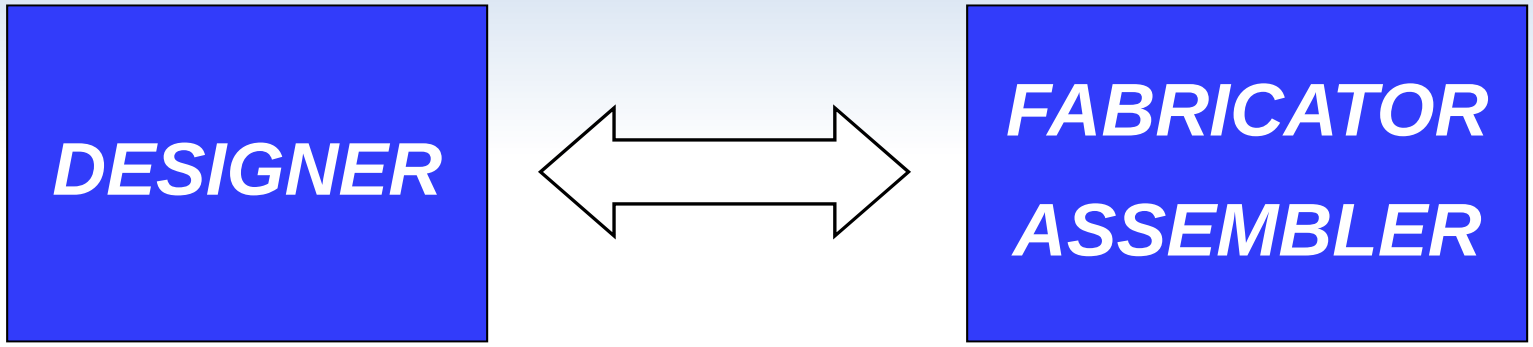
  PROs and CONs
- *Will purchasing select the vendor and if so when?*

  PROs and CONs

Producibility Levels

[IPC-2221A – 1.6.3]

…established to help communicate the design complexity to the manufacturers



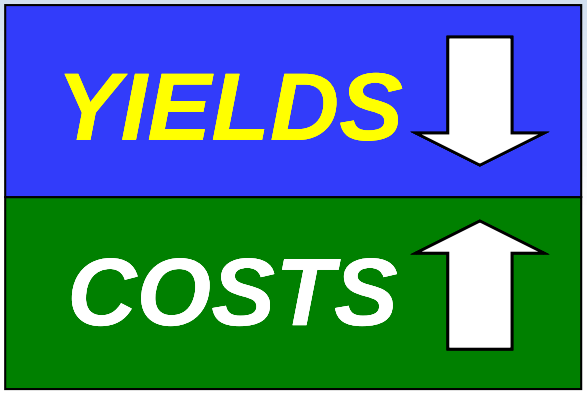
Producibility levels are NOT design requirements

Ask the question, "Is it technologically appropriate for this vendor?"

Producibility Levels

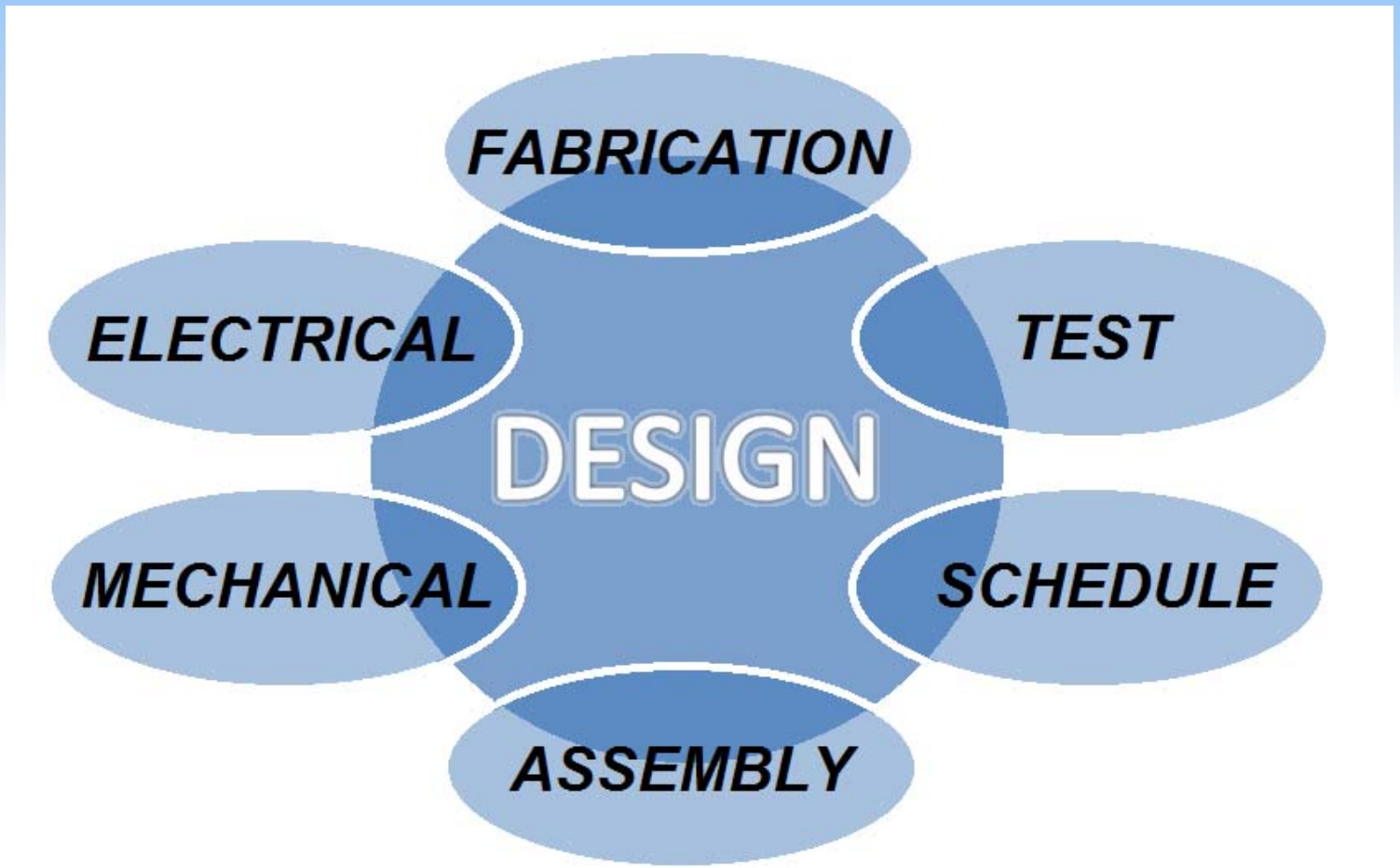
…reflect progressive increases in the sophistication of:

- *tooling*
- *materials*
- *processing*



Hence, progressive increases in fabrication ***cost$***

Who do we collaborate with?

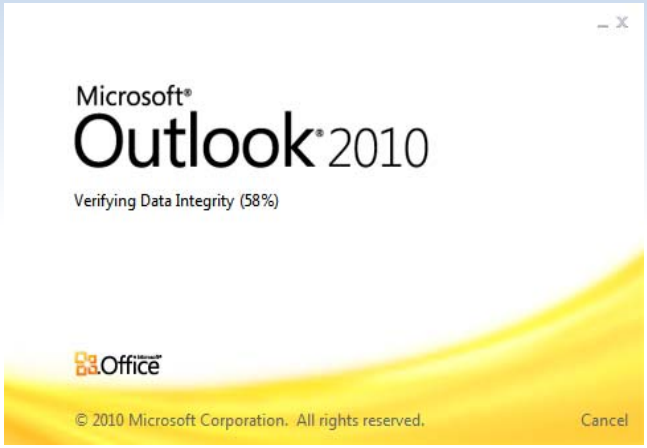


Who do we collaborate with?

Design for Excellence (DFX)

- **DFM - Design for Manufacturing (Fabrication)**
- **DFA - Design for Assembly**
- **DFT - Design for Test**
- **DFR – Design for Reliability**
- **DFE – Design for the Environment**

Making contact should not be optional; it should be standard operating procedure



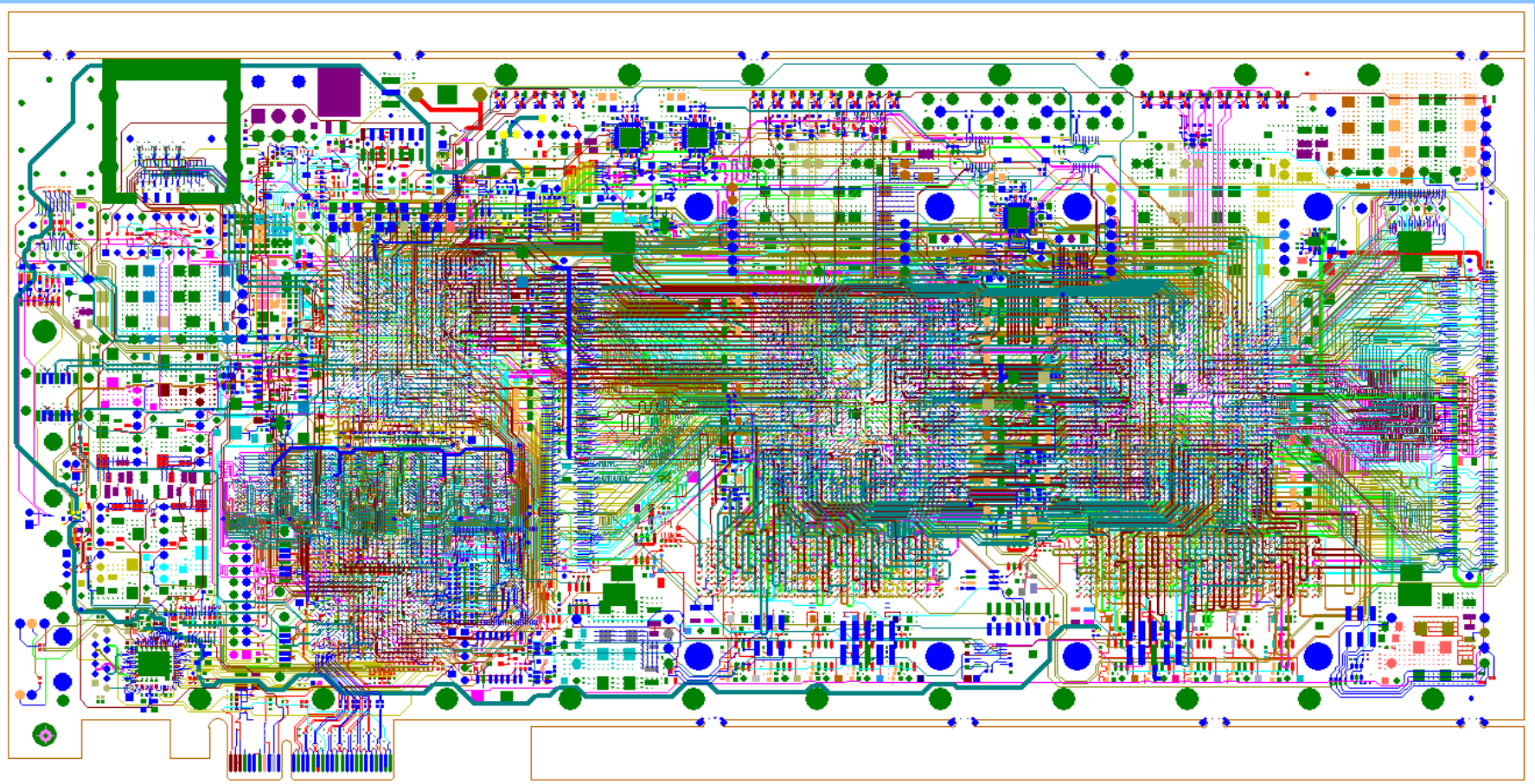
When do we collaborate?

- *When do you communicate to your manufacturing chain?*

  Is it in the 11th hour or is it proactively?
- *When can I get a quote from my fabricator?*
- *When are the feature sizes confirmed?*
- *How and when do you validate your design?*
- *When is the best time for a DFM review?*
- *What is required: Complete or partial data; How about a PO?*

Collaboration should start at the initial estimation of a design!

Board complexities are increasing



*** 18 layers 1.6mm Thk., 10 Ghz, DDR4, 1760 BGA 300 hours, 2 Months**

How would you like to get to this point and then find out it's unbuildable?

Some information you should know at the initial estimation of a design

- Type of end use for a board
  - Build plan High volume production
  - Or is it development or debug
  - Class 2 or Class 3
- Number of I/O signals on a BGA can determine the layer count
- HDI methods allowed
- Feasibility Dispersement Study
- Type of circuitry High-Speed or RF
- Schedule requirements

Challenges have their costs

- *As speed and performance increased, so did the heat*
- *We all know that heat is not our friend…*
- *So voltages had to come down…*
- *As voltage drop, so the size & pitch were reduced…*
- *As performance went up so did the pin count go up…*

Result equaled…

- *Smaller case size*
- *Increased pin count*
- *Lower voltage*
- *Increased thermal*
- *And did I mention…*

"it must cost less and be done faster"!

…Does this mean HDI?

Primary reasons to consider HDI

- *Placement Feasibility – SMT Parts will not fit with room for pin escapes to PTH vias*
- *Standard PTH vias are too large to pin-escape a uBGA (Typically a .65mm or below pitch device)*
- *High Speed or RF performance – unwanted parasitics or excess inductance from standard PTH vias*
- *Increased routing density from high pin count devices. Limited layer count per 1.6mmThk. Bd.*
- *Back to back large active SMT devices – BGA's*
- *RF on Primary Side / Digital on Secondary side*

IC Packaging evolution

Common Land Pitches in Package Family

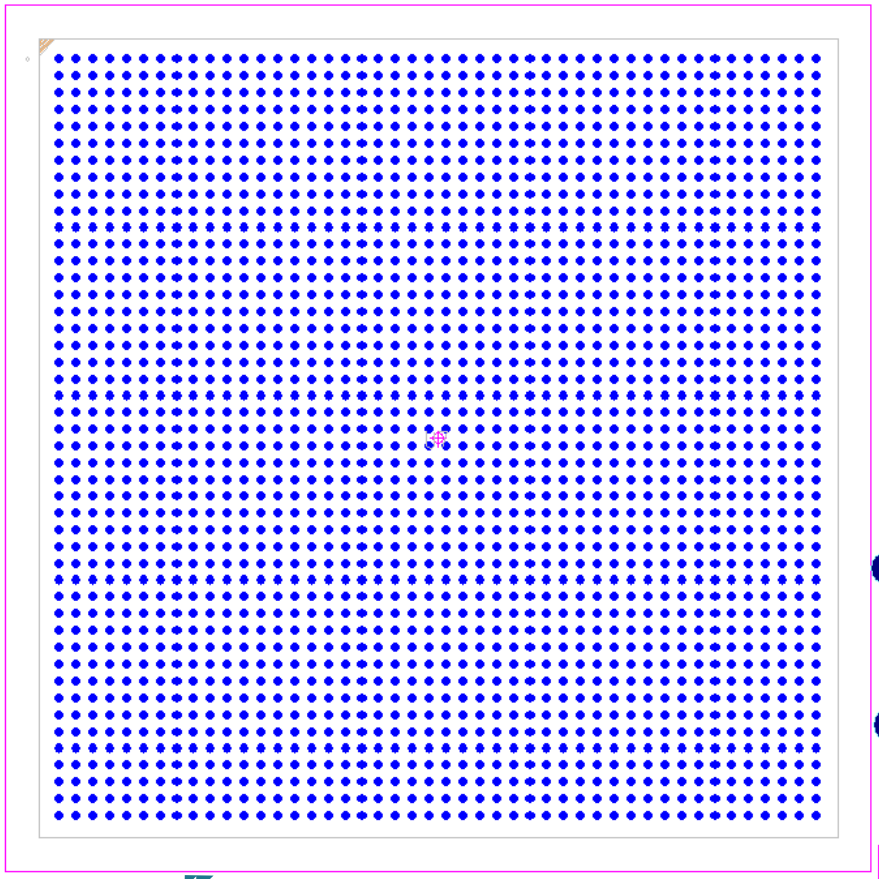
Package type	No. Pins	Description	Peripheral or grid array
SOIC/FQFP	16 - 48	Small outline IC	Peripheral
QFP/PGA/BGA	48 - 156	Quad flat pack/pin grid array/ball grid array	Peripheral and grid array
BGA/QFP	156 - 256	Pitch size 0.5, 0.4, 0.3mm & PGA	Grid array
BGA	> 2000	Large scale integration	Grid array

BGA's ball grid arrays were standardized in the 1990's

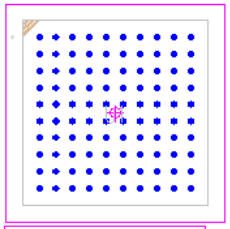
The pin pitch was 1.5 mm [0.060 in], and 1.27 mm [0.050 in]

As smaller and smaller parts evolved they include pitches of 1.0 mm, 0.8, 0.65, 0.5, 0.4, 0.3, and 0.25 mm. (80% rule)

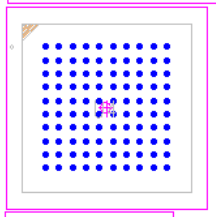
BGA Pin Pitch's (100 pins)



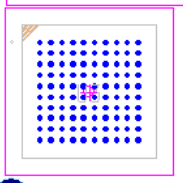
2116 Pin 1.0mm



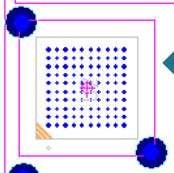
100 Pin
1.0mm



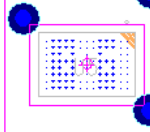
100 Pin
.80mm



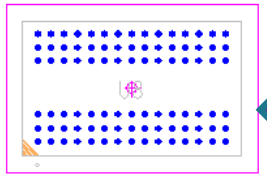
100 Pin
.65mm



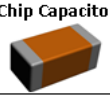
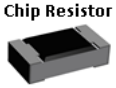
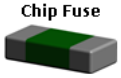
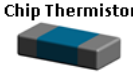
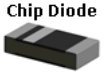
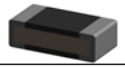
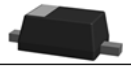
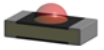
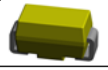
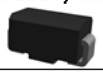
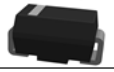
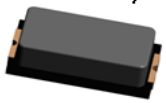
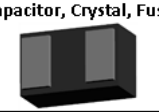
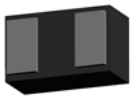
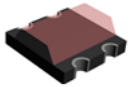
100 Pin
.50mm



100 Pin
.40mm



90 Pin
.80mm
DDR

Chip Capacitor 	Chip Resistor 	Chip Inductor 	Chip Fuse 
Chip Thermistor 	Chip Varistor 	Polarized Chip Capacitor 	Chip Diode 
Chip Non-polarized Diode 	Small Outline Diode (SOD) 	Small Outline Diode Flat Lead 	Chip LED 
Capacitors (CAPM) 	Molded Non-pol Diode 	Fuses (FUSM) 	Molded Body Inductor 
Molded Precision Inductor 	Molded Resistors (RESM) 	Molded Body Polarized Capacitor (CAPMP) 	Molded Body Diode (DIOM) 
Molded Body LED 	MELF Resistor (RESMELF) 	MELF Fuse (FUSEMELF) 	MELF Diode (DIOMELF) 
Aluminum Electrolytic Capacitor 	Crystal 	Side Concave Crystal 	Side Concave Inductor 
DFN Resistor, Inductor, Capacitor, Crystal, Fuse 	DFN Diode and LED 	Diode Side Concave 4-Pin 	LED Side Concave 4-Pin 
SOT23-3 	SOT23-5 	SOT23-6 	SOT23-8 
SOT143 	SOT143 Reverse 	SOT223-4 	SOT223-5 

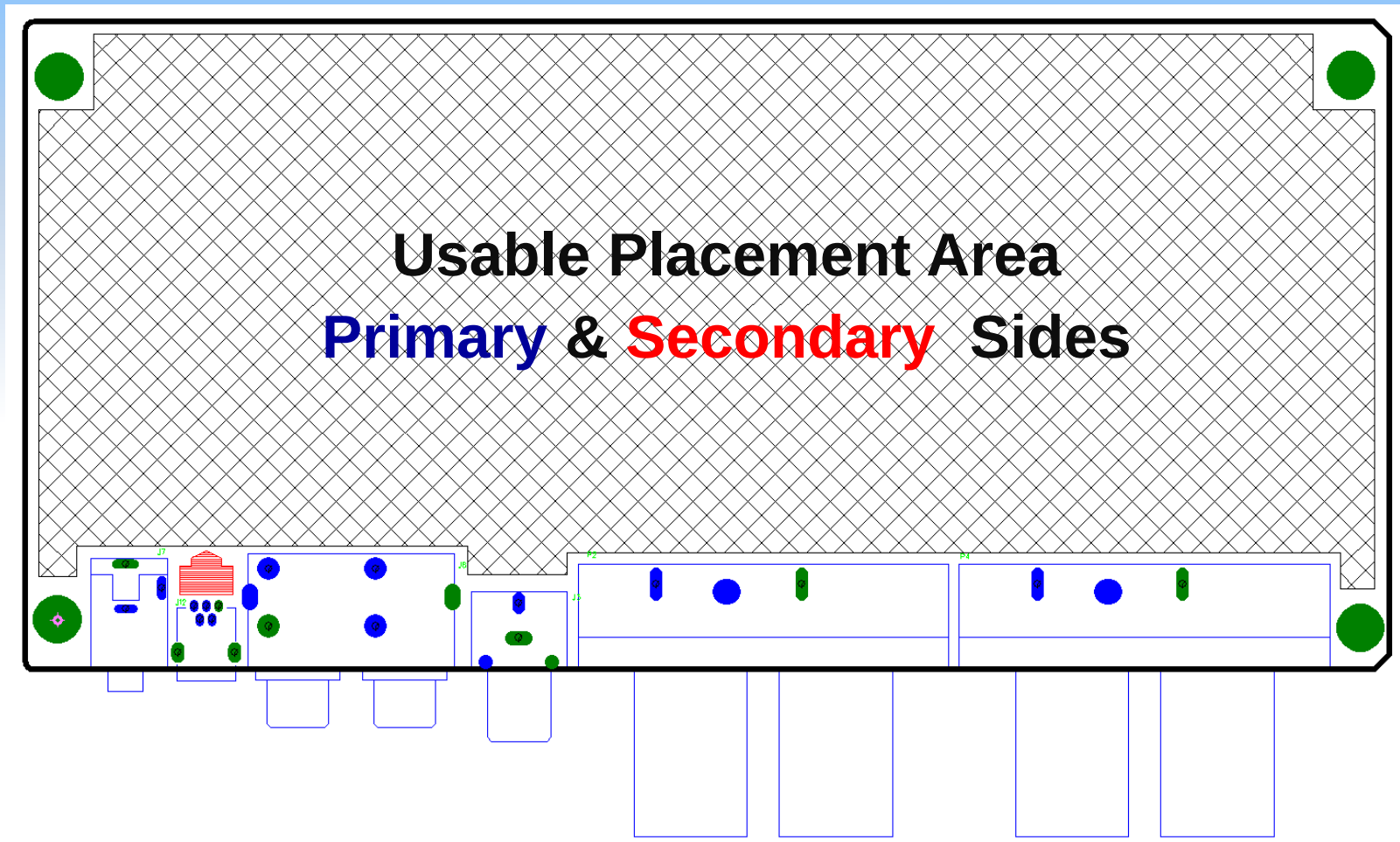
Common Discrete SMT Case

SOT223-6	SOT89	SOTFL 3-Pin	SOTFL 5-Pin
SOTFL 6-Pin	SOTFL 8-Pin	SOTFL 8-Pin	Transistor DFN 3-Pin
Oscillator DFN 4-Pin	Oscillator J-Lead	Oscillator L-Lead	Osc. Corner Concave
Small Outline IC (SOIC)	SOIC with Thermal Tab	Sm Outline Package(SOP)	SOP with Thermal Tab
Ceramic Flat Pack	Quad Flat Package	QFP with Thermal Tab	Ceramic Quad Flat Pack
Small Outline J-Lead	Plastic Lead Chip Carrier	Small Outline L-Lead	Leadless Chip Carrier
Non-collapsing BGA	Collapsing Ball Grid Array	Column Grid Array	Land Grid Array
Small Outline No-lead	SON with Thermal Tab	Quad Flat No-lead	QFN with Thermal Tab
Pull-back Small Outline No-lead	PQFN with Thermal Tab	Pull-back Quad Flat No-Lead	
Concave Chip Array Resistor	Concave Chip Array Inductor	Convex Chip Array Type E	Convex Chip Array Type S

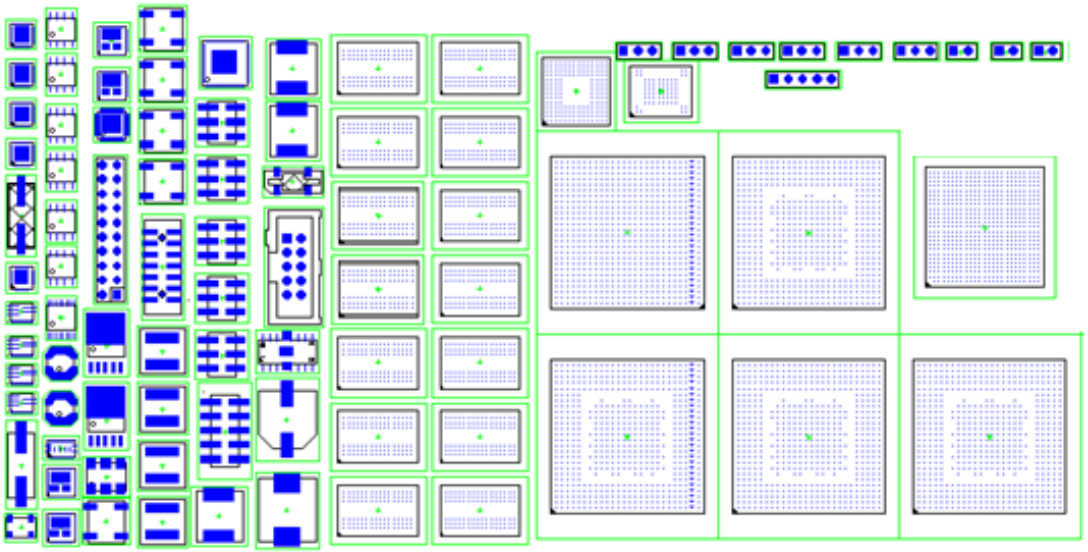
Common Active SMT Case

Images courtesy of PCB Libraries, Inc.

Methods for feasibility

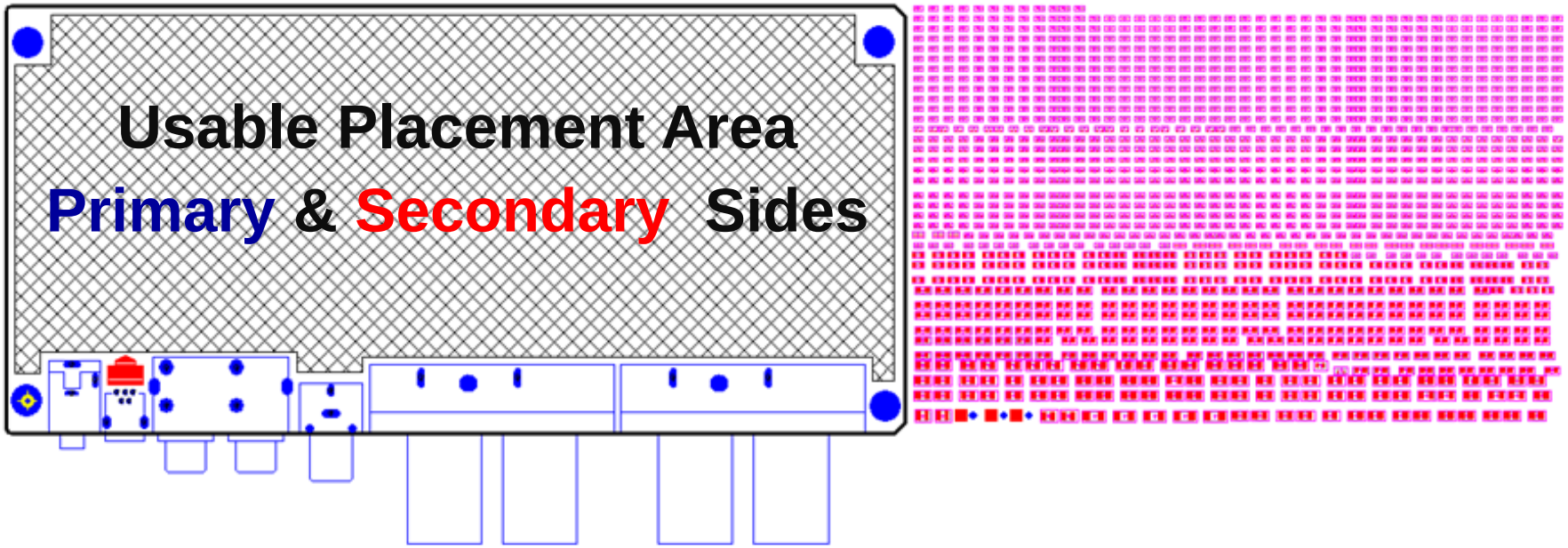


Usable Board Placement Area



Primary Side:
Active Devices
Shown in Blue

Secondary Side:
Passive Devices
Shown in Red



Quick component dispersement shows some feasibility, thus DFM/DFA ready

What do we collaborate?

- *Data: Preliminary and/or Final*
- *Feature sizes*
- *Materials*
- *Capabilities and process adjustments*
- *Build plan and schedule*
- *Process steps vs. turn-time*

Feature sizes for HDI per IPC-2226

Symbol	Feature	Conventional µm [inch]	Threshold µm [inch]	Leading edge µm [inch]	State-of-the-art µm [inch]
a	minimum micro-via size on target land	100 [0.004]	75 [0.003]	75 [0.003]	50 [0.002]
b	maximum micro-via size on capture land	110 [0.004]	80 [0.003]	80 [0.003]	60 [0.002]
c	target land size	350 [0.014]	300 [0.012]	250 [0.010]	130 [0.005]
d	capture land size	350 [0.014]	300 [0.012]	250 [0.010]	130 [0.005]
e	minimum conductor on RDL	125 [0.005]	100 [0.004]	75 [0.003]	50 [0.002]
f	minimum conductor space on RDL	125 [0.005]	100 [0.004]	75 [0.010]	50 [0.002]
g	minimum land with maximum PTH for that land	800 [0.031]	600 [0.024]	400 [0.016]	250 [0.010]
h	minimum PTH diameter	350 [0.014]	250 [0.010]	125 [0.005]	100 [0.004]
i	minimum pitch between micro-vias	1250 [.0049]	800 [0.031]	500 [0.020]	250 [0.010]
j	minimum dielectric thickness RDL	60 [0.002]	50 [0.002]	50 [0.002]	25 [0.001]
k	minimum plating thickness in core vias	25 [0.001]	20 [0.001]	17 [0.001]	17 [0.001]
l	minimum plating thickness in PTH	25 [0.001]	20 [0.001]	17 [0.001]	17 [0.001]
m	minimum plating thickness in micro-via	25 [0.001]	20 [0.001]	17 [0.001]	17 [0.001]
n	minimum board thickness not including plating	800 [0.031]	700 [0.028]	600 [0.024]	600 [0.024]
Important Ratios					
a/j	Maximum aspect ratio for micro-via	0.8	1	1.3	1.5

All copper thicknesses are 17 µm

Plating thickness for 2 to n-1 layer to be nominal 17 µm, minimum 12.5 µm

Annular ring (AR) is land allowance per side of hole. Land diameter equals finished hole size (FHS) + 2x AR.

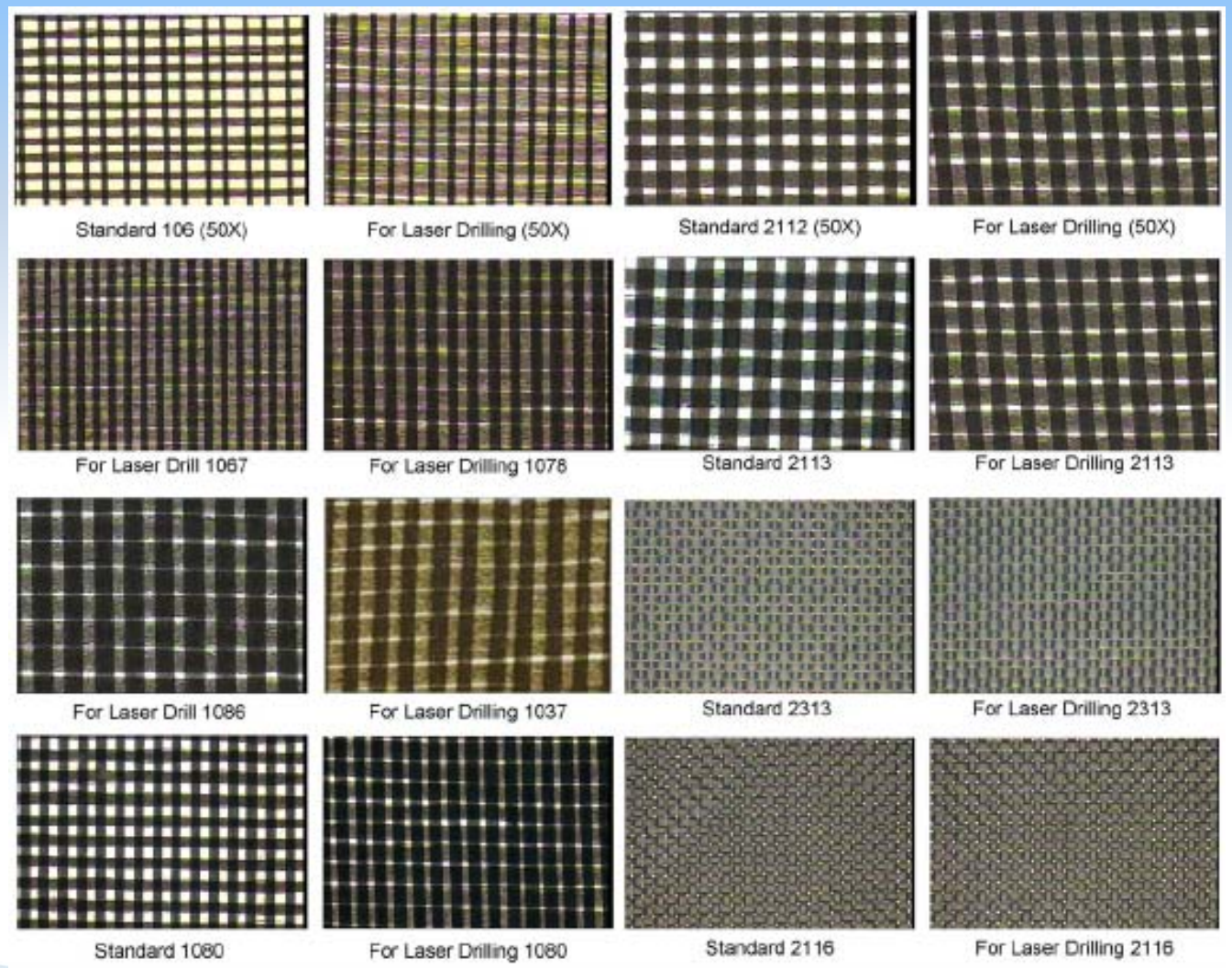
Maximum board thickness requires trade-offs. Contact your supplier

Feature sizes Producibility Levels
IPC-2226

Table 5-1 Typical Feature Sizes for HDI Construction, µm [mil]

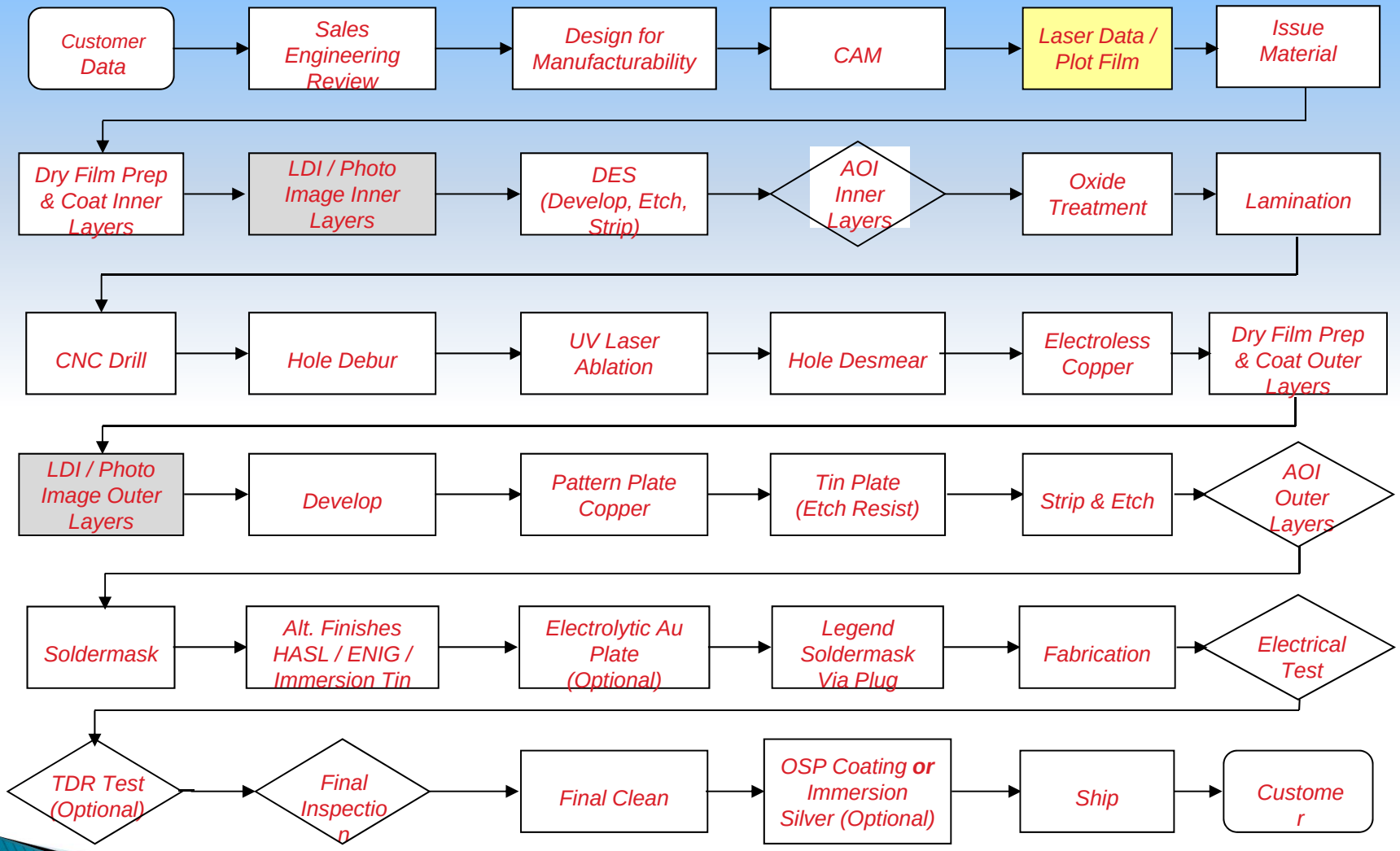
	ASPECT RATIOS	Level A	Level B	Level C
	Microvia plating aspect ratio	≤0.5:1 (k + j) / a	>0.5:1 to 1:1 (k + j) / a	>1:1 (k + j) / a
	Through via hole aspect ratio	≤5:1 (2k + Board Thickness) / h	>5:1 to 9:1 (2k + Board Thickness) / h	>9:1 (2k + Board Thickness) / h
	Buried via aspect ratio	≤5:1 (2r + q) / o	>5:1 to 9:1 (2r + q) / o	>9:1 (2r + q) / o
Symbol	**Feature**	**Level A**	**Level B**	**Level C**
a	Microvia diameter at target land (as formed, no plating)	102 µm [4 mil]	76 µm [3 mil]	51 µm [2 mil]
b	Microvia diameter at capture land (as formed, no plating)	152 µm [6 mil]	127 µm [5 mil]	76 µm [3 mil]
c	Microvia target land size = [(a + 2x annular ring) + FA (1)	406 µm [16 mil]	330 µm [13 mil]	229 µm [9 mil]
	FA for c =	203 µm [8 mil]	152 µm [6 mil]	102 µm [4 mil]
d	Microvia capture land size = [(b + 2x annular ring) + FA (1)]	406 µm [16 mil]	330 µm [13 mil]	229 µm [9 mil]
	FA for d =	203 µm [8 mil]	152 µm [6 mil]	102 µm [4mil]
s	Internal conductor trace width	127 µm [5 mil]	75 µm [3 mil]	50 µm [2 mil]
t	Internal conductor spacing	127 µm [5 mil]	100 µm [4 mil]	50 µm [2 mil]
e	External conductor trace width	127 µm [5 mil]	75 µm [3 mil]	45 µm [1.77 mil]
f	External conductor spacing	127 µm [5 mil]	100 µm [4 mil]	45 µm [1.77 mil]
g	Through via land size = [(h + 2x annular ring width) + FA (1)]	See 9.1.1 of IPC-2221	See 9.1.1 of IPC-2221	See 9.1.1 of IPC-2221

What happens to the quick turn schedule if desired material is not in stock?



…unexpected delays

Do you know your manufacturers typical process flow?



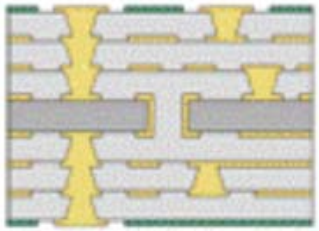
Sequential Lamination Process Flow

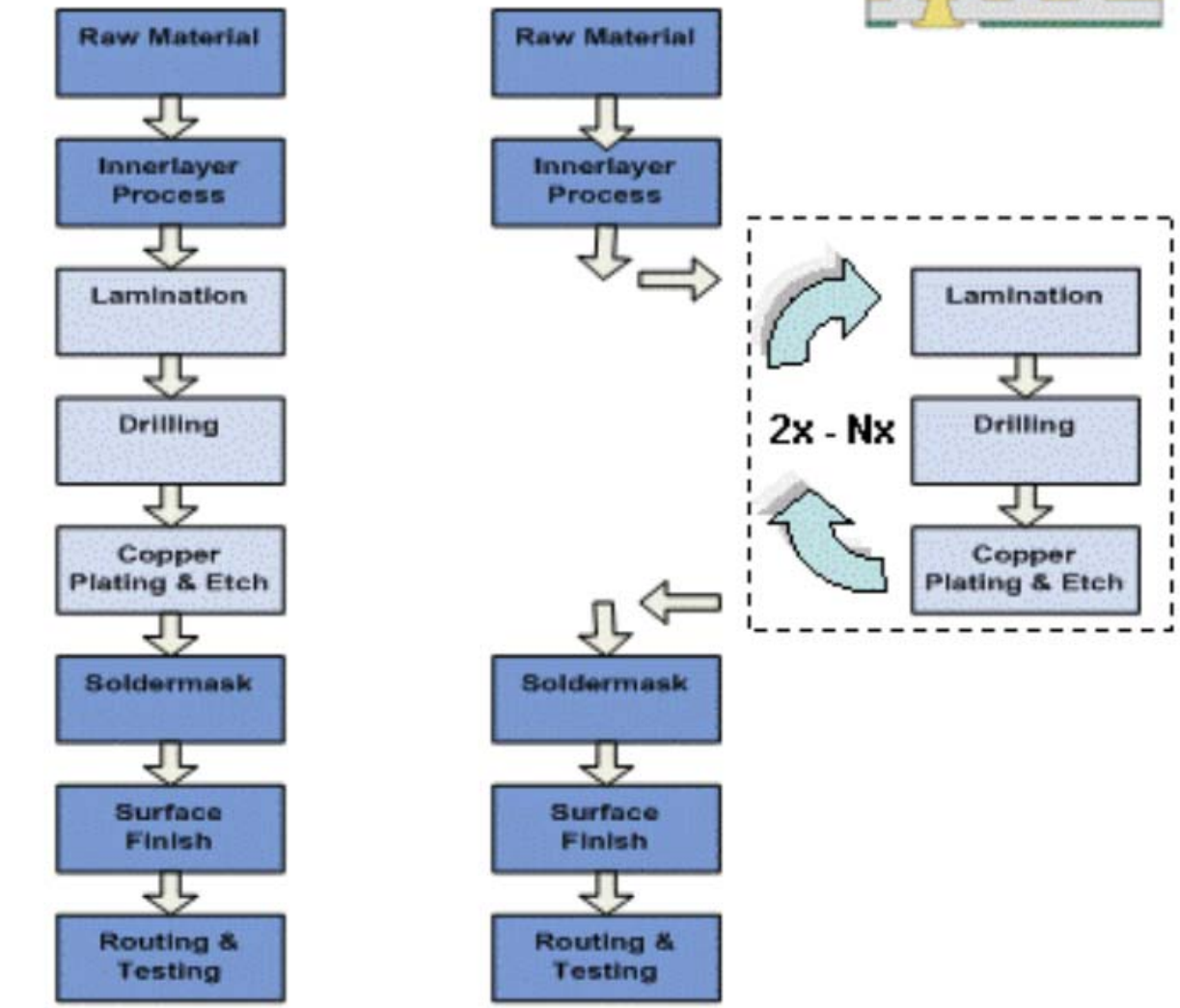
Note the 2x - Nx for build-up of multi-lamination cycles-

Top right image 4 laminations

<u>Process steps can take time!</u>

- Laser Drills
- Copper Filling





What do we collaborate?

- ***Stack-up and impedance:***

  Who's formula or calculator do you use?

  Answer: Whatever you do, consider it a starting point and submit it to the fabricator early.

- ***What material is in stock?***
- ***What are the process adjustments they will use?***
- ***Are the feature sizes and process adjustments good for multiple vendors?***

Stack-up Request: submitted very early in design phase

Please quote and calculate a stack-up for ##14A CAD Design by: San Diego PCB, Inc.
Send it back to Mike.Creeden@sdpcb.com Office (858) 271-5722 www.sdpcb.com

16layer 8”x10”
Material Nelco 4000-13 SI, MEG-6 or equivalent for SERDES 10GHz

Overall board thickness to be 1.6mm (.062) as required.
Surface finish NI/AU
½ OZ CU inners, ¼ OZ outers base CU, plate outers 1.4mil, and plate drill layers as req.
Maybe some heavy CU power planes??

Via in Pad, non-conductive fill, coplanar finish

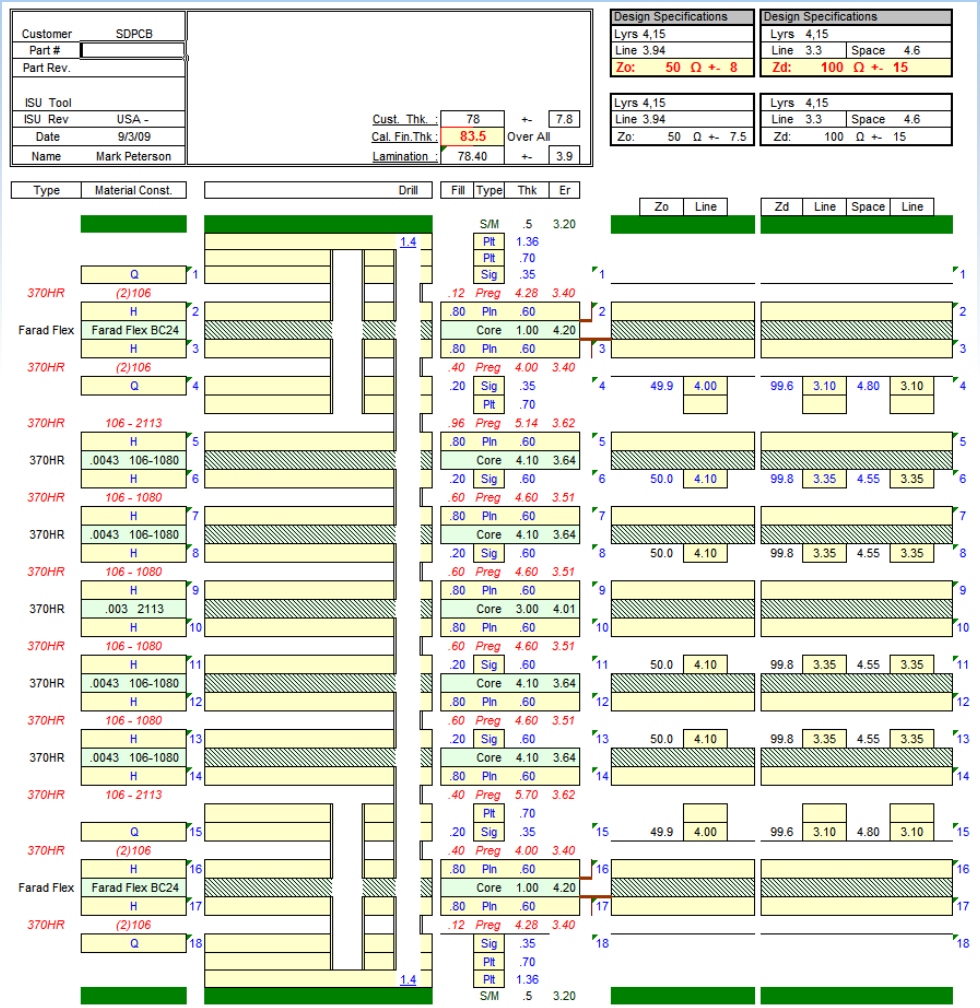
- **Mech. Thru via L1-L16 .5mm pad/.25mmdrill**
- **4-N-4 HDI .010pad/.004 Laser-Via**
- **L5-12 Mechanical “N”-drill 18/8**

Designed features: mostly internal routing
50 ohm +/- 10% .0035 Trace & space inner Layers

100 ohm +/- 10% Differential Pairs - approximately .0033 Trace & space
Routed on [.2mm] pitch center

16 Layer Stack-up Single-Stripline

Layer 1 Top PWR/GND & few traces-via fanout
Layer 2 GND
Layer 3 Signal /PWR
Layer 4 GND
Layer 5 Signal/PWR
Layer 6 GND
Layer 7 Signal /PWR
Layer 8 GND
Layer 9 PWR
Layer 10 Signal/PWR
Layer 11 GND
Layer 12 Signal /PWR
Layer 13 GND
Layer 14 Signal /PWR
Layer 15 GND
Layer 16 Bottom PWR/GND & few traces-via fanout



Designed CLASS 3 or 3A Is it buildable?

- ***The answer to this question can be subjective.***

  The answer is a collaborative result of feature sizes as they relate to manufacturing allowances and process requirements per IPC 2221 and IPC 6012.

- ***Class 3 or Class 3A design (Appendix A, what revision?) (1mil or 2mil Internal Annular Ring) Does the fabricator agree based on our design features, aspect ratio and plating requirements?***

What do we collaborate?

- *What's a panel? Does your Assembly Array provide a good Fabrication Panel utilization or yield?*

  Fab and Assy may be different vendors and have different goals. Collaboration is the key!
- *What are the tolerances in your CAD design data?*

  Answer: None. It's actually True Position data
- *What are the tolerances in your manufactures process?*

  Answer: Many.
- *What is the difference? "Mfg. Process Allowances"*

  How are these documented?
- *How many designers don't understand their own fabrication notes?*

Fabrication notes

SDPCB Fab and Asy Notes
Rev 2.0 as of 12/05/13

Fabrication

NOTES: UNLESS OTHERWISE SPECIFIED; ALL DIMENSIONS ARE IN MM (IN)

1. FABRICATE PCB IAW IPC-4101 AND IPC-6012 USING CUSTOMER SUPPLIED DATA FILES.
A. ALL SPECIFICATIONS TO BE TO THE LATEST STANDARDS.
B. INTERPRET ALL IPC SPECIFICATIONS AS CLASS 2
C. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5-2009 AND/OR IPC-D-325.

2. TOLERANCES:
A. FABRICATE FINISHED BOARD IAW IPC-A-600 AND UL 796(F).
B. HOLE LOCATION TOLERANCE +/-(.075 (.003")) CENTER-TO-CENTER OF TRUE POSITION.
C. ARTWORK REGISTRATION LAYER-TO-LAYER TO BE +/-(.125 (.005")).
D. (1.6 (0.062")) MAXIMUM RADIUS ON ANY INSIDE CORNERS IF REQUIRED.
E. REMOVE ALL BURRS AND BREAK SHARP EDGES (.4 (.016")) MAX (NON-FLEX ONLY).
F. THE FILE <filename>_BD.PHO IS THE BOARD PROFILE FOR THE NC ROUTER.

3. MATERIALS: (1.60 (.062")) +/-10% THICKNESS
A. MATERIAL SHALL BE LAMINATE AND PREPREG IAW IPC-4101/126
B. MATERIAL SHALL HAVE A FLAMMABILITY RATING OF UL 94V-0 OR BETTER.
C. METAL THICKNESS: (UNLESS OTHERWISE SPECIFIED IN LAYER STACKUP)
OUTER LAYERS TO BE (5) OZ CU PLUS 1.0 OZ PLATING FOR 1.5 OZ FINAL THICKNESS.
SIGNAL LAYERS TO BE (5) OZ CU. PLANE LAYERS TO BE (5) OZ CU.
D(RoHS COMPLIANT MATERIALS TO BE USED FOR LEAD-FREE ASSEMBLY PROCESS)

4. FINISH ALL EXPOSED COPPER AREAS: (
.08-.23u (3-6uin) IMMERSION GOLD OVER 3-6u (120-240uin) ELECTROLESS NICKEL.)
A. FABRICATOR MAY APPLY SURFACE FINISH PRIOR TO SOLDER MASK.
B. SOLDER MASK IMAGE AT 1:1 SCALE. FABRICATOR MAY MODIFY SOLDER MASK OTHER THAN SOLDER MASK DEFINED PADS (IF REQUIRED).
C. LIQUID PHOTO IMAGABLE SOLDERMASK PER IPC-SM-840, CLASS (T), BOTH SIDES.
D. COLOR: TRANSPARENT (GREEN) WITH MAX MISREGISTRATION TO BE (.075 (.003")) OVER BARE COPPER. FABRICATOR MAY MODIFY SOLDERMASK IMAGE TO REMOVE ANY SLIVERS THAT ARE (.075 (.003")) OR LESS BETWEEN FINE PITCHED LANDS.
E. ALL PLATED THROUGH HOLES TO HAVE MINIMUM PLATING IAW IPC-6012 TABLE 3.2 AND ALL ANNULAR RINGS TO BE IAW IPC-6012 TABLE 3.5.
F. FABRICATOR MAY ADD TEARDROPS, SHALL REMOVE UNUSED PADS, AND MAY REMOVE ANY CU SLIVERS ON PLANE LAYERS THAT ARE (.075 (.003")) OR LESS

5. MARKING:
A. SILKSCREEN USING (WHITE) EPOXY INK. FABRICATOR MUST MODIFY SILKSCREEN IMAGE TO REMOVE ANY EPOXY INK FROM EXPOSED METAL.
B. FABRICATOR SHALL) DATE CODE IN 4-DIGIT FORMAT (WWYY) AND SHALL) ADD UL ID AS REQUIRED BY UL 796(F) IN SILKSCREEN OR BY STAMP IN AN OPEN AREA OF THE PCB.

SDPCB, Inc. Fabrication and Assembly Notes Rev 2.0 12/05/13 DLC

Comment [DC1]: For Flex ONLY
4204 AND IPC-6013

Comment [DC2]: Solo-Text
Options:
1, 2, 3, 3 WITH VIA CLEARANCE WAIVER

Comment [DC3]: Solo-Text

Comment [DC4]: Solo-Text

Comment [DC5]: Solo-Text

Comment [DC6]: Solo-Text

Comment [DC7]: Solo-Text

Comment [DC8]: Solo-Text
PbFree options
99 370HR 150Tg
121 408 or 408HR 110Tg
124 408HR or I-Speed 150Tg
126 370HR 170Tg
129 408HR or I-Speed 170Tg

PbOption
21 408 or 408HR 110Tg
24 370HR, 408HR, or I-Speed 150Tg
26 370HR or 406 170Tg

Comment [DC9]: Solo-Text

Comment [DC10]: Solo-Text

Comment [DC11]: Solo-Text

Comment [DC12]: Solo-Text
D. NON RoHS COMPLIANT MATERIALS OK.
If changed, degrade slash sheet to a Pb Option

Comment [DC13]: Options
Cost Adder: ENIG $.18/sqin or $25/panel min. $75/order min

PbFree options:
.15-.5u (6-20uin) IMMERSION SILVER
1-1.5u (40-60uin) IMMERSION TIN
MINIMUM 2.5u (100uin) Pb-FREE HASL
Cost Adder: $15/panel
.05-.2u (2-8uin) IMMERSION GOLD OVER .05-.38u (2-15uin) ELECTROLESS PALLADIUM OVER 3-6u (120-240uin) ELECTROLESS NICKEL

Pb Option:
MINIMUM 2.5u (100uin) Tin-Lead HASL
Cost Adder: $15/panel

Comment [DC14]: AS SEEN ON <DESIGNATOR>

Comment [DC15]: Solo-Text. Options:
T – Telecommunications
H - High reliability

Comment [DC16]: Solo-Text. Options:
CLEAR, BLUE, RED, YELLOW, ORANGE, WHITE, BLACK

Comment [DC17]: Solo-Text

Comment [DC18]: Solo-Text

Comment [DC19]: Solo-Text

Comment [DC20]: Solo-Text. Options:
YELLOW, BLACK

Comment [DC21]: MAY

Comment [DC22]: MAY

6. TEST REQUIREMENTS:
A. ALL BOARDS TO PASS 100% CONTINUITY TEST FOR OPENS AND SHORTS USING SUPPLIED IPC-D-356 NETLIST.)
B. FABRICATOR SHALL) PERFORM DWV (HIPOT) TEST PER IPC-TM-650.
C. REFER TO TABLE FOR FINAL (CHARACTERISTIC IMPEDANCE) VERIFICATION OF IMPEDANCE BY MEANS OF TDR IS REQUIRED. FABRICATOR MAY MODIFY DESIGNED TRACE WIDTH AND DIELECTRIC THICKNESS FOR ETCH LOSS AND MATERIAL DIFFERENCES. LOWER END OF IMPEDANCE TOLERANCE IS ACCEPTABLE TO PROVIDE WIDER TRACE. TRACES THAT TRAVEL OVER MINIMAL GAPS ON SPLIT PLANE LAYERS ARE ACCEPTABLE. FABRICATOR TO PROVIDE THE FINAL STACKUP INFORMATION TO CUSTOMER.
D. PERMANENTLY MARK PASSED BOARDS IN AN OPEN AREA.

7. PANELIZATION:
A. IF NO PANELIZATION IS SPECIFIED, FABRICATOR TO PROVIDE ASSEMBLY HANDLING RAILS PER ASSEMBLY REQS INCLUDING TOOLING, FIDUCIALS, BREAK-AWAYS, ETC.
B. PANELIZATION IS TO FAVOR STD V-SCORE OVER RATBITES WHENEVER POSSIBLE.
C. IF MULTIPLE-UP PANELIZATION IS PERFORMED, FABRICATOR TO PROVIDE THE EDITED MULTIPLE-UP SOLDER PASTE GERBER FILES TO ASSEMBLER AND/OR TO CUSTOMER.

8. THIEVING:
A. FABRICATOR MAY ADD THIEVING TO COMPENSATE FOR LOW COPPER DENSITY AREAS.)
B. THIEVING TO BOARD EDGE SPACING 2.5 (.100") MINIMUM.
C. THIEVING TO FIDUCIAL SPACING 5.0 (.200") MINIMUM.
D. THIEVING TO NON-PLATED THROUGH HOLES 5.0 (.200") MINIMUM.
E. THIEVING TO ALL OTHER FEATURES .25 (.010") MINIMUM.
F. THERE SHALL BE NO THIEVING IN ANY AREA FREE OF SOLDERMASK.

9. ADDITIONAL NOTES:)
(VIA IN PAD) FABRICATOR MUST ADD NON-CONDUCTIVE EPOXY FILL, SURFACE PLATE, COPLANAR SURFACE FINISH FOR ALL DRILL SIZES OF (.25)
EDGE FINGERS:) ELETRO-PLATE EDGE CONN HARD GOLD OVER LOW STRESS NICKEL.
RIGID FLEX:
A. FLEX BASE IAW IPC-4204 USING POLYIMIDE (PI).)
B. ADHESIVE IAW IPC-4203.
C. COVERLAY FLEX SECTIONS IAW IPC-4203 IF APPLICABLE.
D. APPLY BLACK ECOBOND 45 AT ALL FLEX TO RIGID JUNCTIONS IF APPLICABLE.
()

Assembly

NOTES: UNLESS OTHERWISE SPECIFIED
1. WORKMANSHIP PERFORMED IAW IPC-A-610 AND/OR J-STD-001.
A. ALL SPECIFICATIONS TO BE TO THE LATEST STANDARDS.
B. INTERPRET ALL IPC SPECIFICATIONS AS CLASS 2)
C. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5-2009 AND/OR IPC-D-325.
2. RoHS COMPLIANT MATERIALS TO BE USED FOR LEAD-FREE ASSEMBLY PROCESS.)
3. COMPONENT MOUNTING PER IPC-CM-770.

SDPCB, Inc. Fabrication and Assembly Notes Rev 2.0 12/05/13 DLC

Comment [DC23]: Solo-Text
PER FABRICATOR STANDARD TEST.

Comment [DC24]: MAY

Comment [DC25]: Cost Adder: 5%

Comment [DC26]: Option:
A. NO THIEVING ALLOWED
Delete B-F is option is used

Comment [DC27]: Left on L25 in blocks to add in if necessary.

Comment [DC28]: Cost Adder: $65/panel

Comment [DC29]: Solo-Text

Comment [DC30]: Cost Adder: $50/panel most cases. More fingers means more cost.

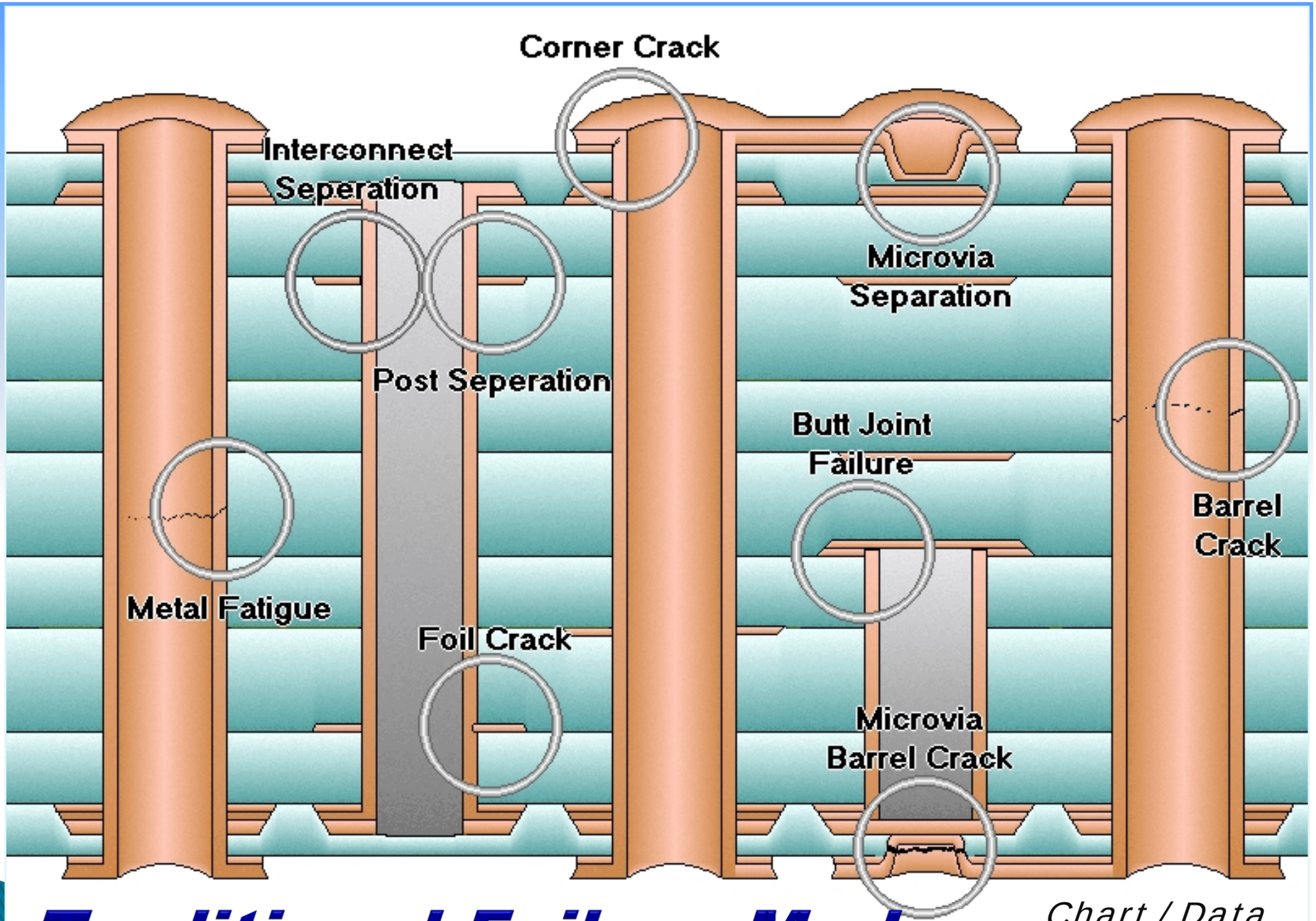
Comment [DC31]: Solo-Text. Options:
POLYESTER (PET).
POLYETHYLENE NAPTHALATE (PEN).
POLYETHERIMIDE (PEI).

Comment [DC32]: Additional Cost Adders:
Extra layer pairs i.e.4 layer up to 6 layers: 10%
Blind Vias: 25%/set
Buried Vias: 15%/set
Filled Vias: $30/panel
Slots: 10%
Smallest Hole Size: 3-30% based on aspect ratio starting at 12:1
Hole Count: 3-10% based on holes/sqin starting at 100

Comment [DC33]: Solo-Text

Comment [DC34]: Solo-Text
2. NON RoHS COMPLIANT MATERIALS OK.

A Responsible PCB Designer or Engineer should understand these notes as they relate to their board



Traditional Failure Modes

Chart / Data Courtesy PWB Interconnect

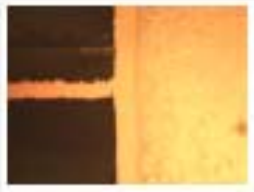
Happy Halloween.jpg

Horizontal section - separations into t...

Missing plating.jpg

Nodule.jpg

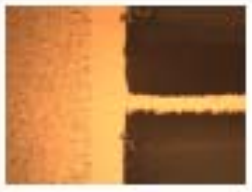
Nodules and smear.jpg



Partial Smear prior to etching.jpg

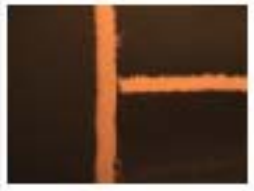
Partial Smear sample after etching.jpg

Separation at the interconnect aft...

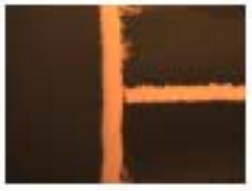


Separation at the interconnect prior ...

Separation.jpg

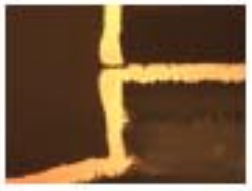


Smear at the interconnect aft...



Smear at the interconnect prior ...

Thin copper plating.jpg



void in plating.jpg

Stacked Vias

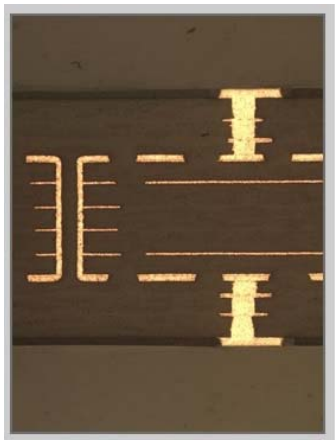
Defects found in vias through micro-sectioning

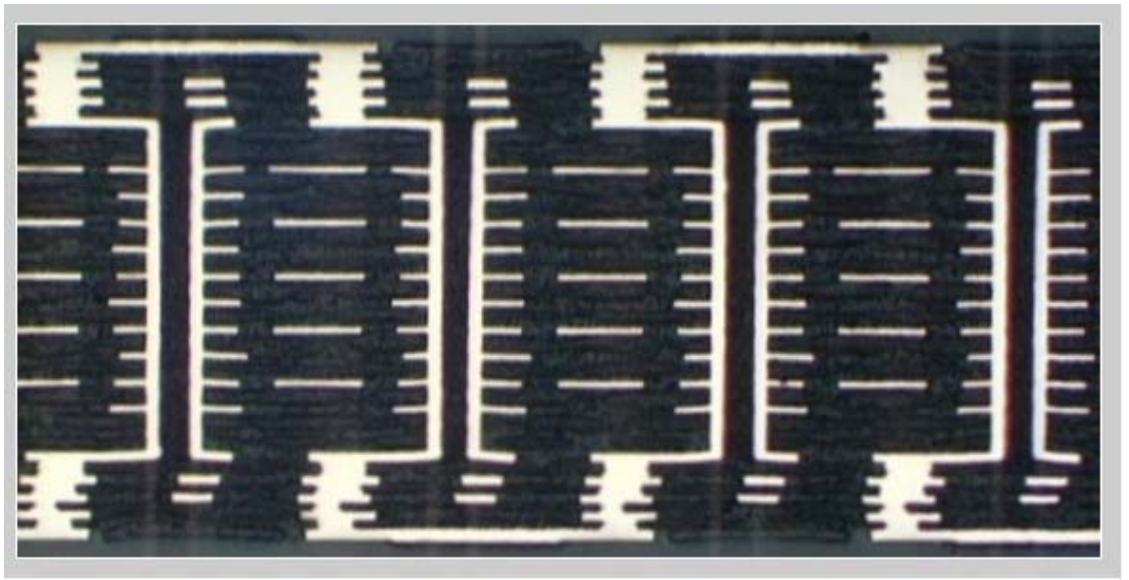
Stacked micro vias

Stacking of laser vias:

Tests have shown that multiple stacked laser vias are stable due to the thinner dielectrics and the plated fill.

However, it is not recommended to stack laser vias on top of mechanical buried vias; due to the epoxy fill which creates dissimilar Z-Axis CTE issues.





IST & HATS Testing

IST Tester
Interconnect Stress

HATS™ Tester
Highly Accelerated Thermal Shock

Best way to have good test results is to design for high yield manufacturing via collaboration.

Summary

- *We want a board that would function and perform well.*
- *We also want to have a high manufacturing yield to our build, thus lowering cost.*
- *Collaborating with your manufacturing team through the entire layout phase is the best way to design a "correct by construction" circuit.*
- *The best solution to any problem is to preclude it!*

Remember IPC is not a "THEM", it's an "US"!

Thank you, very much!

Michael R. Creeden CEO/CID+
San Diego PCB, Inc.
mike.creeden@sdpcb.com
(858)271-5722

SAN DIEGO PCB, INC.